The Examiner issues new grounds of rejection relating to claim amendments filed in the last response. The Examiner objects to the claim amendments under 35 U.S.C. §132, and alleges that it introduces new matter into the disclosure. The Examiner also rejects claims 1-20 under 35 U.S.C. §112, first and second paragraphs. The Examiner alleges that the newly claimed subject matter is not described in the specification, and that the claims fail to particularly point out and distinctly claim the invention. The Examiner states even further that claims 1, 11, 19, and 21 are misdescriptive rendering the claims indefinite. We respectfully disagree.

Rejections under 35 U.S.C. §132 and 35 U.S.C. §112, first and second paragraphs

A point of the Examiner's misinterpretations seems to be focused on the timing diagram of Figs. 4 and 5 of the application. The Examiner opines that the main power-on detection signal (/POROH) is active from activation of a second activating power-on detection signal, which does not correspond to the illustrations or description of the subject application. It seems that the Examiner takes the position that when main power-on detection signal /POROH attains a high level (H-level), the state corresponds to an "active state." The Examiner also takes the position that it is not explicitly illustrated that the main power-on detection signal /POROH attains a L-level at the inactivation of a second activated power-on detection signal, as claimed.

As defined throughout the specification, an H-level (high level) of the power-on detection signal corresponds an "inactive state" and an L-level (low level) corresponds to an "active state." There is no requirement known to the Applicants that a H-level must correspond to an active state, as the Examiner interprets the claim. Since the Examiner has interpreted the claims in an opposite manner, we believe that the new matter and §112 rejections have been made in error, especially when the claims are read in light of the specification.

In particular, referring to the specification, on page 9, lines 16-31, it is stated that the power-on detection circuit 10 detects the power-on of the logic power supply voltage VDDL and holds a power-on detection signal /POROL "at an active state" while the logic power supply voltage VDDL is unstable (L-level). This state corresponds to time Tc to Td illustrated by Fig. 4. The cited text of the application also explains that the power-on detection signal /POROH is held "at the active state L-level" until the power supply voltage VDDH becomes stable, which corresponds to time Ta to time Tb as also illustrated by Fig. 4. Hence, the main power-on detection signal /POROH is at the active state (L-level) when at least one of the power-on detection signals is active, which corresponds up until time Td, as illustrated by Fig. 4. As the application explicitly states, "when both of the power supply voltages VDDL and VDDH attain the stable state, the main power-on detection signal /POROH enters the H-level inactive state."

Adverting to the claims, amendments were made generally to each of independent claims 1, 11, 19, and 20.

Claim 1 recites, *inter alia*:

> a main power-on detection circuit coupled to the first and second power-on detection circuits for generating a main power-on detection signal rendered active from activation of a first activated power-on detection signal of the first and second power-on detection signals until inactivation of a second activated power-on detection signal of the first and second power-on detection signals.

As the specification thoroughly explains, the main power-on detection signal is active from activation of a first activated power-on detection signal until inactivation of a second power-on detection signal. As Figs. 4 and 5 illustrate, the main power-on detection signal is at an active state (L-level) from Ta to Td (Fig. 4) or Te to Th (Fig. 5). As illustrated, when a second power-on detection signal inactivates (changes to H-level), so does the main power-on detection signal. The amendments conform to the illustrations and description. Hence, no new matter has been entered,

and moreover, the claims are supported by the specification and particularly point out and distinctly claim the invention.

Amendments to claims 11, 19, and 20 entered in the last response are as follows:

Claim 11 recites, *inter alia*:

> a main power-on detection signal rendered active from activation of a first activated detection signal of the internal voltage power-up detection signal and the power-on detection signal until inactivation of second activated detection signal of internal voltage power-up detection signal and the power-on detection signal.

Claim 19 recites, *inter alia*:

> for activating a main power-up detection signal from activation of a first activated power-up detection signal in the power-up detection signals until inactivation of a last activated power-up detection signal in the power-up detection signals, to hold an internal circuit in a reset state.

Claim 20 recites, *inter alia*:

> a main power-on detection signal made active from activation of a first activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal until inactivation of a last activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal, to hold an internal circuit in a reset state.

Claims 11, 19, and 20, although not identical to the amendment to claim 1, generally recite the conditions by which the main power-on detection signal is made active. Each of the claims conform to the illustrations and description, as does claim 1.

Applicants respectfully request that the objection under 35 U.S.C. §132 and the rejection under 35 U.S.C. §112, first and second paragraphs, are withdrawn. The Examiner is encouraged to contact Applicants undersigned representative, if the Examiner needs further assistance in understanding the amended claim language in light of the figures in the description.

It is further submitted that claims 1, 11, 19, and 21 are not misdescriptive, as the Examiner has alleged. As discussed above, the claims clearly conform to the figures and description.

Rejection Under 35 U.S.C. §102

The Examiner maintains the same positions with respect to claims 1-3, 7, and 19 as in the last response.

As to claim 1, however, the Examiner seems to take a somewhat more limited position that Fig. 6 (instead of Figs. 6 and 9) of Crotty discloses the claimed subject matter. As to Fig. 6 of Crotty, the Examiner continues to maintain that buffer circuit 650 reads on the claimed main power-on detection circuit of claim 1. We respectfully disagree.

Col. 9 of Crotty, as the Examiner references, describes the embodiment incorporating voltage detection circuit 630 in parallel with dual-voltage detection circuit 210 of Fig. 2.

As explained in the last response, Crotty intends to prevent malfunction of the internal logic circuit in uncertain or indefinite state of the input signal due to insufficient voltage applied to the input/output circuit, and in particular, intends to prevent the signal/data transfer between input/output circuits and the internal circuit when the first power supply voltage is at an insufficient level and the second power supply voltage is at a sufficient level. This is accomplished by a power-on reset circuit for dual-voltage logic devices, which is configured to reset an internal circuit upon a power-on condition. Particularly, the first power supply voltage Vcc1 is supplied to the input/output circuit and the second power supply voltage Vcc2 is supplied to the internal logic circuit. Dual detection circuit 210 determines whether Vcc1 is greater than a predetermined voltage. When the voltage level of the first power supply voltage Vcc1 is insufficient, the internal circuit receiving the second power supply voltage for operation is reset. Therefore, Crotty is directed to detection of a single power application sequence. Specifically, when the first power supply voltage is applied while the second power supply

voltage is not applied, the power on reset signal POR is activated, as shown in Figs. 3(b), 3(d), and Fig. 8 of Crotty.

Voltage detection circuit 630 is coupled between power supply Vcc2 (also supplied to voltage detection circuit 210) and a ground voltage. Circuit 630 detects whether Vcc2 is less than adequate voltage Vad2.

Both of voltage detection circuits 210 and 630 are coupled to buffer circuit 650. It is emphasized that buffer circuit 650 is provided to remove spurious noise which may cause an inadvertent reset.

Buffer circuit 650 outputs a power-on reset signal POR, which is in the power-off logic level, if power supply voltage Vcc1 is less than adequate voltage Vad1, or if supply voltage Vcc2 is less than adequate voltage Vad2 for longer than a transient period of time. (See col. 9, line 20-24). In other words, when either power-on reset signal POR1 or POR 2 attain a logic high level, output signal POR remains at a logic-low level. Only when power supply voltages Vcc1 and Vcc2 are adequate does POR attain an active logic-high level. The following table lists the various states of signal POR relative to input signals POR1 and POR2.

	POR1	**POR2**	**POR**
1.	0 (inactive)	0 (inactive)	0 (inactive)
2.	0 (inactive)	1 (active)	0 (inactive)
3.	1 (active)	0 (inactive)	0 (inactive)
4.	1 (active)	1 (active)	1 (active)

As the above table illustrates, POR attains an active state with both POR1 and POR2 are active.

As can be seen from the table, "activation of a first activated power-on detection signal of the first and second power-on detection signals", as claim 1 recites, would correspond any one of rows 2 and 3. "Until inactivation of a second activated power-on detection signal of the first and second power-on detection signals", as claim 1 recites, would correspond to any one of rows 1, 2, and 3. Contrary to claim 1, in the period between these states, POR of Crotty remains at an inactive state. Nowhere does Crotty disclose or suggest that POR is "rendered active from activation of a first activated power-on detection signal of the first and second power-on detection signals until inactivation of a second activated power-on detection signal of the first and second power-on detection signals", as claim 1 recites.

Applicants maintain the same position with respect to independent claim 19. Claim 19 recites, *inter alia*, "for activating a main power-up detection signal from activation of a first activated power-up detection signal in the power-up detection signals until inactivation of a last activated power-up detection signal in the power-up detection signals, to hold an internal circuit in a reset state." Again, "activation of a first activated power-up detection signal" would correspond to any one of rows 2 and 3. "Until inactivation of a last activated power-up detection signal" would correspond to row 1. Contrary to claim 19, as can be seen from the above table, POR maintains inactivate during the conditions.

Claims 2, 3, and 7, cited under the rejection, are patentable based at least on their dependency to any one of claims 1 and 19 and for the reasons discussed above. For the above reasons, withdrawal of the anticipation rejection of claims 1-3, 7, and 19 is respectfully solicited.

Rejection Under 35 U.S.C. §103

The Examiner maintains the rejection by references Fig. 9 of Crotty. The Examiner acknowledges that Crotty does not disclose the claimed internal voltage generation circuit, but

states that it would have been obvious to use a voltage step-down circuit to generate the reduced voltage. The Office Action states further that it would have been obvious to use the step-down circuit for generating the internal voltage Vcc1 ... "if the design value of the internal voltage is higher than a voltage level which the circuit provides." We respectfully disagree.

Claim 11 is patentable over the Crotty reference as Crotty fails to disclose or suggest the main power-on detection circuit, as set forth above.

Claim 11 recites "a main power-on detection circuit responsive to said internal voltage power-up detection signal and said power-on detection signal for generating a main power-on detection signal rendered active from activation of a first activated detection signal of the internal voltage power-up detection signal and the power-on detection signal until inactivation of second activated detection signal of internal voltage power-up detection signal and the power-on detection signal."

The OR gate 950 of the low pass filter 930, which removes transient signal levels, is incapable of functioning as the claimed main power-on detection circuit, as suggested and for the reasons set forth above. Moreover, the state of the POR signal of Crotty in relation to activation/inactivation of signals POR1 and POR2 does not read on the language of claim 11. The Examiner is referred to the discussion above under the anticipation rejection.

Claim 20 recites "main power-on detection circuit responsive to said at least one internal voltage power-up detection signal and said at least one power-on detection signal for generating a main power-on detection signal made active from activation of a first activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal until inactivation of a last activated detection signal in said at least one power-up detection signal and said at least one power-on detection signal, to hold an internal circuit in a reset state."

The claimed main power-on detection circuit is neither disclosed nor suggested by Crotty, for the same reasons discussed in relation to claim 11. Additionally, there is no disclosure or suggestion of the low pass filter or OR gate holding an internal circuit in a reset state, as claimed. Moreover, the state of the POR signal of Crotty in relation to activation/inactivation of signals POR1 and POR2 does not read on the language of claim 20. The Examiner is again referred to the discussion above under the anticipation rejection.

Claims 16 and 18, cited under the rejection, are patentable based at least on their dependency to any one of claims 11 and 20 and for the reasons discussed above. For the above reasons, withdrawal of the obviousness rejection of claims 11, 16, 18, and 20 is respectfully solicited.

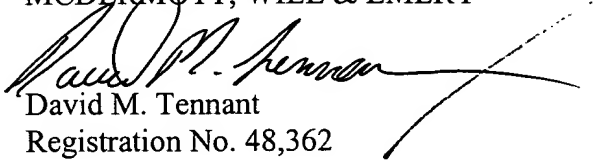
Conclusion

In light of the remarks above, this application should be considered in condition for allowance and passed to issue. If there are any questions regarding this response or the application in general, a telephone call to the undersigned representative would be appreciated to expedite prosecution of this case.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY



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